REMARKS

In the Office Action, the Examiner rejected claims 1, 2, 10-13, 19, 23, and 24 and indicated that claim 22 would be allowable if rewritten in independent form. Applicants thank the Examiner for indicating the allowability of claim 22 and have rewritten claim 22 in independent form as new claim 25. By this paper, Applicants have cancelled claims 22 and 24 without prejudice. In view of the remarks set forth below, Applicants respectfully request reconsideration and allowance of all pending claims.

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 11-13, 23 and 24 were rejected as being unpatentable under Section 103 based on Lopez-Aguado (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820). Claims 10 and 19 were rejected under Section 103 based on Lopez-Aguado in view of Shiell and further in view of Handy. With respect to claims 1, 2, 11-13, 23 and 24, the Examiner stated:

> 4. Claims 1-2, 11-13 and 23-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado et al. (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820). Regarding claims 1 and 23, Lopez-Aguado discloses a processor having a normal mode (normal mode occurs during cache hits) and a speculative prefetching mode (speculative mode occurs during prefetch cache hits when the prefetch bit is not asserted and when data cache misses occur, the processor operable in the speculative prefetching mode after a data cache miss comprising a first data cache for storing data when the processor operates in the normal mode (Figure 3, Reference 105; C6, L57-60) - inherently data is stored in cache 105 when a cache write hit occurs); and a second data cache for storing data in response to a store instruction only when the processor operates in the speculative prefetching mode (Figure 3, Reference 106; C6, L27-54; C6, L60-67; C7, L1-67); a first program counter for use when the processor operates in the normal mode (C4, L10-11; C5, L57-61; Figure 7, Reference 300). Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode. However,

Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C2, L24-36). This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.

Regarding claim 2, Lopez-Aguado and Shiell disclose the second data cache containing an entry for storing data (Lopez-Aguado - Figure 5), Reference DATA); and a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary (invalid) data (Lopez-Aguado - Figure 5, Reference INV).

Regarding claims 11-12 and 24, Lopez-Aguado discloses a processor having a normal mode and a speculative prefetching mode, wherein the processor operates in the speculative prefetching mode after a data cache miss occurs comprising a first register/first cache (a cache is random access memory comprised of registers, the first register consists of one of the registers in cache 105 in Figure 3) for storing data during the normal mode (normal mode occurs during data cache hits to Reference 105 of Figure 3; inherently data is stored in cache 105 when a cache write hit occurs); a second register/second data cache (the second register consists of one of the registers in cache 106 in Figure 3) for storing data only during the speculative prefetching mode (C6, L27-54; C6, L60-7; C7, L1-67); speculative prefetching mode occurs during prefetch cache hits when the PREFETCH bit is un-asserted [C6, L60-67; C7, L1-67] and after data cache misses [C6, L27-54] and data is stored in the second register only during the speculative prefetching mode), the second register comprising a first trash bit that indicates whether the second register contains arbitrary data (Figure 5, Reference INV); an instruction bus for receiving a stream of instructions including a first instruction and a second instruction (Figure 4, Reference 128; C4, L22-28); control logic for executing the first instruction (C6 , L10-13) - primary pipeline for executing the first instruction having an un-asserted LP bit); control logic for initiating a cache fill request provided execution of the first instruction encounters a data cache miss (C6, L34-48); control logic for setting the trash bit of the second register in response to the first instruction and

the data cache miss (C6, L34-54); control logic for executing the second instruction in the speculative prefetching mode using the second register in place of the first register (C4, L22-34; C5, L57-67; C6, L1-4, L18-23 - when a data request (instruction) corresponding to an asserted LP bit is paired with a data request (instruction) corresponding to an un-asserted LP bit, a first request having an un-asserted LP bit is executed via the primary pipeline and accesses the data cache while the second request having an asserted LP bit is executed via the secondary pipeline and accessing the prefetch cache in place of the data cache); a first program counter for use when the processor operates in the normal mode (C4, L10-11; C5 , L57-61; Figure 7, Reference 300). Lopez-Aguado does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during the operation of the processor in the speculative prefetching mode. However, Shiell teaches the concept of providing a first program counter for use when a processor operates in a first mode and a second program counter for use when a processor operates in a second mode wherein the first counter is configured to remain unchanged during the operation of the processor in the second mode (C2, L 24-36). This feature taught by Shiell provides efficient control logic by separating the operation of the program counters for each mode of operation, which intrinsically simplifies the control logic for controlling the program counter operations for the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Shiell with the system taught by Lopez-Aguado for the desirable purpose of efficiency.

Regarding claim 13, Lopez-Aguado and Shiell disclose the second data cache containing an entry for storing data (Lopez-Aguado - Figure 5, Reference DATA); and a trash bit associated with the entry, wherein the trash bit indicates whether the entry contains arbitrary (invalid) data (Lopez-Aguado - Figure 5, Reference INV).

Office Action, pages 2-5.

With respect to claims 10 and 19, the Examiner stated:

5. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado (USPN: 6,317,810) in view of Shiell (USPN: 6,317,820) as applied to

> claims 1 and 11 above and further in view of Handy, The Cache Memory Book.
>
> Lopez-Aguado and Shiell disclose the second data cache as an associative cache (Lopez-Aguado - C4, L46-50), however, Lopez-Aguado does not disclose the first cache as a direct mapped cache. Handy teaches that direct mapped caches are the simplest most common way to design a cache (Lopez-Aguado - Page 54, Paragraph 1, last two lines). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Lopez-Aguado's first cache as a direct mapped cache for the desirable purpose of simplification.
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> Office Action, pages 5-6.

Applicants respectfully traverse these rejections. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Claims 1, 2, and 10

Turning now to claims, independent claim 1 recites, among other things, a processor comprising "a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode." In the Office Action, the Examiner correctly notes that the Lopez-Aguado reference "does not explicitly disclose a second program counter for use only when the processor operates in the speculative prefetching mode." Page 3, lines 3-5. In an attempt to cure this deficiency, the Examiner suggested that the Shiell reference discloses this feature. *See* page 3, lines 7-16.

For at least two reasons, the Shiell reference, however, does not disclose a second program counter for use only when the processor operates in the speculative pre-fetch mode. First, the Shiell reference does not even disclose the existence of a speculative prefetching mode, much less a processor operating in the speculative prefetching mode, as reciting in claim 1. In fact, the Shiell reference never uses the word "speculative," and the one use of the word "prefetching" in the Shiell reference is clearly a reference to conventional prefetching and not the speculative prefetching mode recited in claim 1. *See* col. 9, lines 14-16. For this reason alone, the Examiner should withdraw the rejection of independent claim 1.

Second, even ignoring the complete absence of a speculative prefetching mode in the Shiell reference, the program counters disclosed in the Shiell reference clearly do not anticipate claim 1. The Shiell reference is directed towards a "very long instruction word data processor including plural data registers, plural functioning units, and plural program counters." Shiell, col. 2, lines 24-26. These plural data registers, plural functional units, and plural program counters permit the processor disclosed in Shiell to operate in a "split" mode

wherein "the data processor fetches N/2 bits of instructions corresponding to the first program counter and fetches N/2 bits of instructions corresponding to the second program counter." Shiell, col. 3, lines 11-14, col. 6, lines 25-48. This "split" mode permits the processor to process two independent program instructions simultaneously. Shiell, col. 2, lines 44-46. Because the processor disclosed in Shiell clearly uses both program counters simultaneously while processing programmed instructions in split mode, it cannot disclose "a second program counter for use only when the processor operates in speculative prefetching mode, wherein the *first program counter is configured to remain unchanged* during operation of the processor in speculative prefetching mode," as recited in independent claim 1 (emphasis added). For this additional reason Applicants respectfully requests that the Examiner withdraw the rejection of independent claim 1 and the claims that depend therefrom.

Claims 11-13, 19, and 23

Independent claim 11 recites, among other things, a processor comprising "a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode." As with the rejection of independent claim 1, the Examiner correctly noted in the Office Action that the Lopez-Aguado reference does not disclose this feature and, as such, relies on the Shiell reference to cure this deficiency. Page 5, lines 5-16. For reasons very similar to those stated above with regard to independent claim 1, it is clear that the Shiell reference does not disclose this feature. As described above, the Shiell reference does not disclose either a speculative prefetching mode or a second program counter for use only when the processor operates in the speculative prefetching mode, wherein the first program counter is configured to remain unchanged during operation of the processor in the speculative prefetching mode. For these reasons,

Applicants respectfully request withdraw of the § 103(a) rejections against independent claim 11 and the claims that depend therefrom.

Claims 10 and 19

Applicants respectfully submit that claims 10 and 19 are allowable based on their dependencies on claims 1 and 11 because the Handy reference does not cure the deficiencies in the Lopez-Aguado reference and the Shiell reference. For this reason, claims 10 and 19 are allowable for the reasons outlined above. Thus, Applicants respectfully request withdrawal of the 103(a) rejections against claims 10 and 19 and allowance of all pending claims.

Conclusion

In view of the remarks set forth above, Applicants respectfully request withdrawal of all of the Examiner's rejections. Furthermore, Applicants assert that an indication of the allowability of claims 1, 2, 10-13, 19, 23, and 25 is appropriate. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: November 22, 2004

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